AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-46 (Cancelled).

47. (Original) A method for fabricating a microtransformer comprising the steps of:

providing a substrate with at least a first and second through-holes that define between them a coil winding area that includes a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes;

forming a first layer of magnetic material on said substrate in said coil winding area; and

forming a first layer of electrically conductive material forming at least one coil winding on said substrate in said coil winding area.

48. (Original) The method of claim 47, wherein said first layer of electrically conductive material has two coils.

49. (Original) The method of claim 47 further comprising the step of providing a first insulating layer between said first layer of magnetic material and said substrate.

50. (Original) The method of claim 49 further comprising the step of providing a second insulating layer between said first layer of magnetic material and said layer of electrically conductive material.

51. (Original) The method of claim 50 further comprising the step of providing a top protective insulating layer over said first layer of electrically conductive material.

52. (Original) The method of claim 51 further comprising the step of providing a passivating layer over said top protective insulating layer.

53. (Original) The method of claim 50 further comprising the step of forming a second layer of magnetic material over said first layer of electrically conductive material.

54. (Original) The method of claim 53 further comprising the step of providing a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

55. (Original) The method of claim 54 further comprising the step of forming a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

56. (Original) The method of claim 55 further comprising the step of forming an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

57. (Original) The method of claim 55 further comprising the step of providing a top protective insulating layer over said second layer of electrically conductive material.

58. (Original) The method of claim 57 further comprising the step of providing a passivating layer over said top protective insulating layer.

59. (Original) A system-on-chip comprising:

a substrate having a through-hole microtransformer formed thereon; and

at least one integrated circuit chip attached to said substrate and electrically connected to said substrate.

60. (Original) The system-on-chip of claim 59, wherein said through-holes microtransformer is formed in a coil winding area defined by first and second through-holes in said substrate, said coil winding area including a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes.

61. (Original) The system-on-chip of claim 59, wherein said microtransformer further comprises a first layer of magnetic material provided on said substrate in said coil winding area and a first layer of electrically conductive material forming at least one coil winding provided on said substrate in said coil winding area.

62. (Original) The system-on-chip of claim 61, wherein said layer of electrically conductive material forms two coil windings.

63. (Original) The system-on-chip of claim 62, wherein said two coil windings form a primary and secondary coil windings of said microtransformer.

64. (Original) The system-on-chip of claim 61, wherein said microtransformer further comprises a first insulating layer between said substrate and said first layer of magnetic material.

65. (Original) The system-on-chip of claim 64, wherein said microtransformer further comprises a second insulating layer formed between said first layer of magnetic material and said first layer of electrically conductive material.

66. (Original) The system-on-chip of claim 65, wherein said microtransformer further comprises a top protective insulating layer over said first layer of electrically conductive material.

67. (Original) The system-on-chip of claim 66, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

68. (Original) The system-on-chip of claim 65, wherein said microtransformer further comprises a second layer of magnetic material formed over said first layer of electrically conductive material.

69. (Original) The system-on-chip of claim 68, wherein said microtransformer further comprises a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

70. (Original) The system-on-chip of claim 69, wherein said microtransformer further comprises a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

71. (Original) The system-on-chip of claim 70, wherein said microtransformer further comprises an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

72. (Original) The system-on-chip of claim 71, wherein said microtransformer further comprises a top protective insulating layer over said second layer of electrically conductive material.

73. (Original) The system-on-chip of claim 72, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

74. (Original) The system-on-chip of claim 59, wherein said at least one chip contains analog circuitry.

75. (Original) The system-on-chip of claim 59, wherein said at least one chip contains digital circuitry.

76. (Original) The system-on-chip of claim 59 further comprising a power supply on said substrate.

77. (Original) The system-on-chip of claim 59 further comprising a DC-DC converter on said substrate.

78. (Original) The system-on-chip of claim 59, wherein said substrate is a semiconductor substrate.

79. (Original) The system-on-chip of claim 78, wherein said semiconductor substrate is a silicon substrate.

80. (Original) The system-on-chip of claim 78, wherein said semiconductor substrate is a germanium substrate.

81. (Original) The system-on-chip of claim 78, wherein said semiconductor substrate is a gallium arsenide substrate.

82. (Original) The system-on-chip of claim 59, wherein said substrate is a quartz substrate.

83. (Original) The system-on-chip of claim 59, wherein said substrate is a ceramic substrate.

84. (Original) The system-on-chip of claim 59, wherein said substrate is a Al_2O_3/TiC substrate.

85. (Original) A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a through-hole microtransformer, said microtransformer being formed in a coil winding area defined by a first and second through-holes in a substrate, said coil winding area including a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes.

86. (Original) The processor-based system of claim 85, wherein said microtransformer further comprises a first layer of magnetic material provided on said substrate in said coil winding area and a first layer of electrically conductive material forming at least one coil winding provided on said substrate in said coil winding area.

87. (Original) The processor-based system of claim 86, wherein said microtransformer further comprises a first insulating layer formed between said substrate and said first layer of magnetic material.

88. (Original) The processor-based system of claim 87, wherein said microtransformer further comprises a second insulating layer formed between said first layer of magnetic material and said first layer of electrically conductive material.

89. (Original) The processor-based system of claim 88, wherein said microtransformer further comprises a top protective insulating layer over said first layer of electrically conductive material.

90. (Original) The processor-based system of claim 89, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

91. (Original) The processor-based system of claim 88, wherein said microtransformer further comprises a second layer of magnetic material formed over said first layer of electrically conductive material.

92. (Original) The processor-based system of claim 91, wherein said microtransformer further comprises a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

93. (Original) The processor-based system of claim 92, wherein said microtransformer further comprises a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

94. (Original) The processor-based system of claim 93, wherein said microtransformer further comprises an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

95. (Original) The processor-based system of claim 94, wherein said microtransformer further comprises a top protective insulating layer over said second layer of electrically conductive material.

96. (Original) The processor-based system of claim 95, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

97. (Original) The processor-based system of claim 85, wherein said integrated circuit is part of a memory circuit.

98. (Original) The processor-based system of claim 85, wherein said substrate is a semiconductor substrate.

99. (Original) The processor-based system of claim 98, wherein said semiconductor substrate is a silicon substrate.

100. (Original) The processor-based system of claim 98, wherein said semiconductor substrate is a germanium substrate.

101. (Original) The processor-based system of claim 98, wherein said semiconductor substrate is a gallium arsenide substrate.

102. (Original) The processor-based system of claim 85, wherein said substrate is a quartz substrate.

103. (Original) The processor-based system of claim 85, wherein said substrate is a ceramic substrate.

104. (Original) The processor-based system of claim 85, wherein said substrate is a Al_2O_3/TiC substrate.